

Features

- FAX and Modem interface (V.34/V.34+)
- Designed to work at data rates up to 56kbits
- External programmable line and network balance impedances
- Programmable DC termination characteristics
- IEC950 recognised component
- Transformerless 2-4 Wire conversion
- Integral Loop Switch
- Dial Pulse and DTMF operation
- Accommodates parallel phone detection
- Line state detection outputs:
-loop current/ringing voltage/line voltage
- +5V operation, low on-hook power (25mW)
- Full duplex voice and data transmission
- On-Hook reception from the line
- Meets French current limit requirements
- Conforms to German dial pulse standards
- Approvable to UL 1950

Applications

Interface to Central Office or PABX line for:

- FAX/Modem
- Electronic Point of Sale

ISSUE3

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Package Information

MH88437AD-P 28 Pin DIL Package
MH88437AS-P 28 Pin SM Package

0°C to 70°C

- Security System
- Telemetry
- Set Top Boxes

Description

The Mitel MH88437 Data Access Arrangement (D.A.A.) provides a complete interface between audio or data transmission equipment and a telephone line. All functions are integrated into a single thick film hybrid module which provides high voltage isolation, very high reliability and optimum circuit design, needing a minimum of external components.

The impedance and network balance are externally programmable, as are the DC termination characteristics, making the device suitable for most countries worldwide.

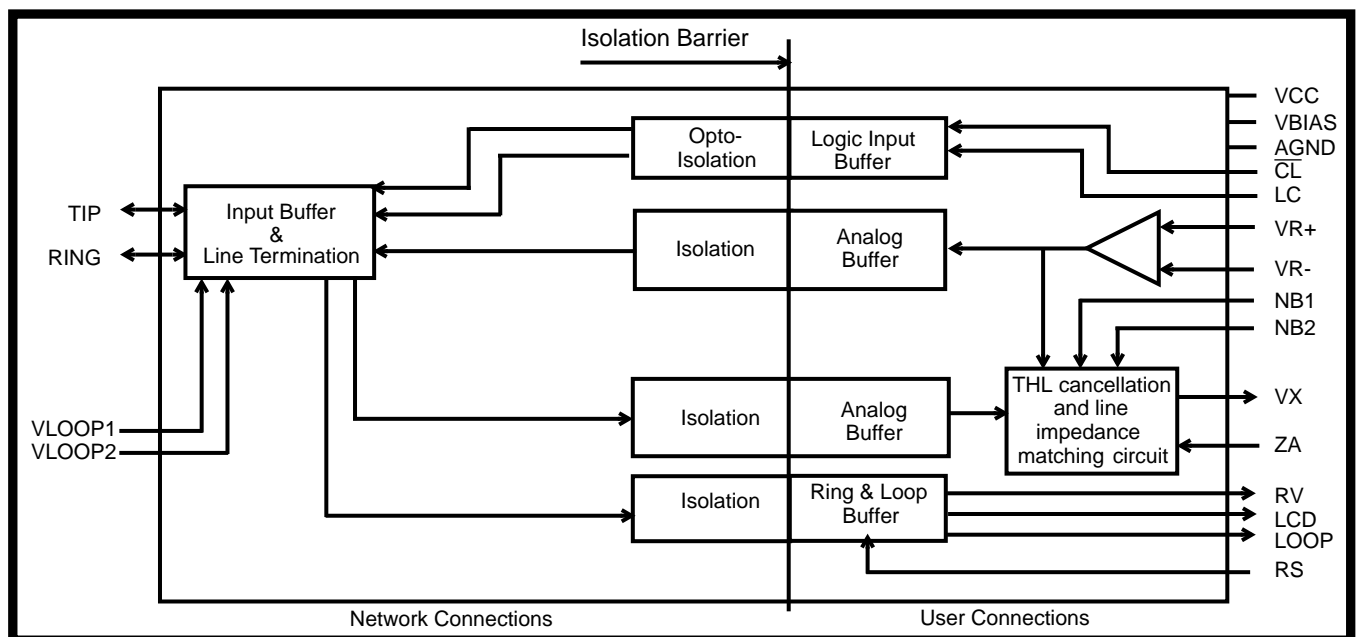


Figure 1 - Functional Block Diagram

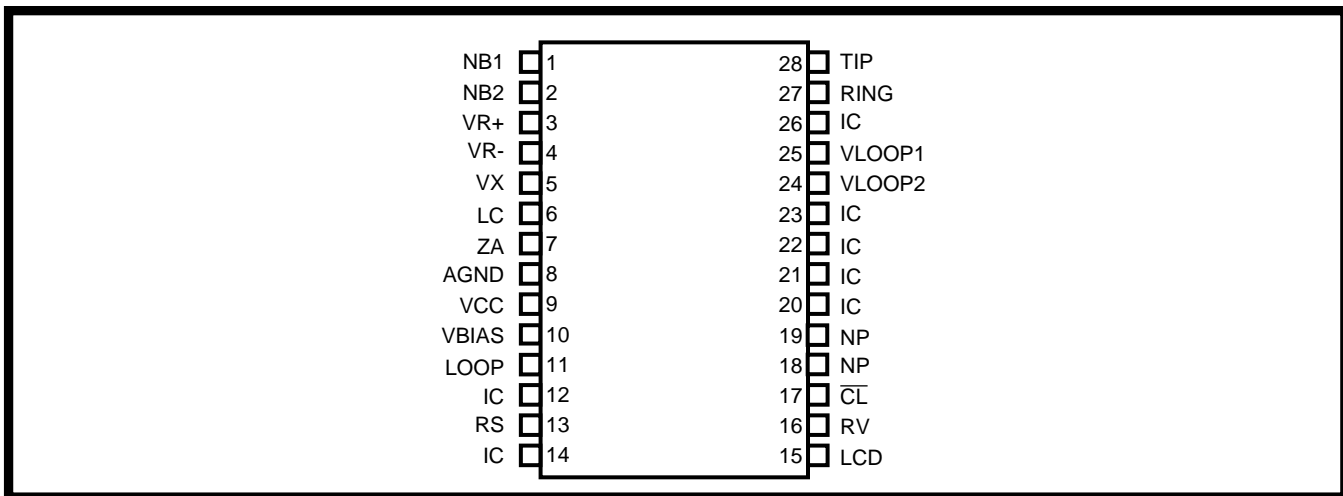


Figure 2 - Pin Connections

Pin Description

Pin #	Name	Description
1	NB1	Network Balance 1. External passive components must be connected between this pin and NB2.
2	NB2	Network Balance 2. External passive components must be connected between this pin and NB1.
3	VR+	Differential Receive (Input). Analog input from modem/fax chip set.
4	VR-	Differential Receive (Input). Analog input from modem/fax chip set.
5	VX	Transmit (Output). Ground referenced (AGND) output to modem/fax chip set, biased at +2.0V.
6	LC	Loop Control (Input). A logic 1 applied to this pin activates internal circuitry which provides a DC termination across Tip and Ring. This pin is also used for dial pulse application.
7	ZA	Line Impedance. Connect impedance matching components from this pin to Ground (AGND).
8	AGND	Analog Ground. 4-Wire 0V reference connect to mains earth (ground). See MSAN 154 for applications with no earth (ground) connection.
9	V _{CC}	Positive Supply Voltage. +5V.
10	VBIAS	Internal Reference Voltage. +2.0V reference voltage. This pin should be decoupled externally to AGND, typically with a 10 μ F 6.3V capacitor.
11	LOOP	Loop (Output). The output voltage on this pin is proportional to the line voltage across Tip - Ring, scaled down by a factor of 50.
12, 14	IC	Internal Connection. No connection should be made to this pin externally.
13	RS	Ringing Sensitivity. Connecting a link or resistor between this pin and LOOP (pin 11) will vary the ringing detection sensitivity of the module.
15	LCD	Loop Condition Detect (Output). Indicates the status of loop current.
16	RV	Ringing Voltage Detect (Output). The RV output indicates the presence of a ringing voltage applied across the Tip and Ring leads.
17	CL	Current Limit. A logic 0 applied to this pin activates internal circuitry which limits the loop current.
18	NP	No Pin. Isolation Barrier, fitted, no pin fitted in this position.

Pin Description (continued)

Pin #	Name	Description
19	NP	No Pin. Isolation barrier, no pin fitted in this position
20,21 22,23 26	IC	Internal Connection. No connection should be made to this pin externally.
24	VLOOP2	Loop Voltage Control Node 2. Used to set DC termination characteristics.
25	VLOOP1	Loop Voltage Control Node 1. Used to set DC termination characteristics.
27	RING	Ring Lead. Connects to the "Ring" lead of the telephone line.
28	TIP	Tip Lead. Connects to the "Tip" lead of the telephone line.

Functional Description

The device is a Data Access Arrangement (D.A.A.). It is used to correctly terminate a 2-Wire telephone line. It provides a signalling link and a 2-4 Wire line interface between an analog loop and subscriber data transmission equipment, such as Modems, Facsimiles (Fax's), Remote Meters, Electronic Point of Sale equipment and Set Top Boxes.

Isolation Barrier

The device provides an isolation barrier capable of meeting the supplementary barrier requirements of the international standard IEC 950 and the national variants of this scheme such as EN 60950 for European applications and UL 1950 for North American applications.

External Protection Circuit

An External Protection Circuit assists in preventing damage to the device and the subscriber equipment, due to over-voltage conditions. See Application Note MSAN-154 for recommendations.

Suitable Markets

The MH88437 has features such as programmable line and network balance impedance, programmable DC termination and a supplementary isolation barrier. For countries that do not need to meet the French and German requirements there is a pin for pin compatible device the MH88435.

There are, however, a small number of countries with a 100M Ω leakage requirement that this device does not meet. These are Belgium, Greece, Italy, Luxembourg, Spain and Poland. Although

Luxembourg will now accept TBR21 and there are exceptions to the Italian specification, in most applications the MH88437 will comply with Luxembourg and Italian specifications. For approval in Denmark and Sweden the TRB21 route is recommended.

Approval specifications are regularly changing and the relevant specification should always be consulted before commencing design.

Line Termination

When Loop Control (LC) is at a logic 1, a line termination is applied across Tip and Ring. The device can be considered off-hook and DC loop current will flow. The line termination consists of both a DC line termination and an AC input impedance. It is used to terminate an incoming call, seize the line for an outgoing call, or if it is applied and disconnected at the required rate, can be used to generate dial pulses.

The DC termination resembles approximately 300 Ω resistance, which is loop current dependent. Furthermore, it can be programmed to meet different national requirements. For normal operation VLOOP3 should be open circuit and a resistor (R2) should be fitted between VLOOP1 and VLOOP2, as shown in Figure 4.

The approval specification will give a DC mask characteristic that the equipment will need to comply to. The DC mask specifies the amount of current the DAA can sink for a given voltage across tip and ring. Graph 1 shows how the voltage across tip and ring varies with different resistors (R2) for a given loop current.

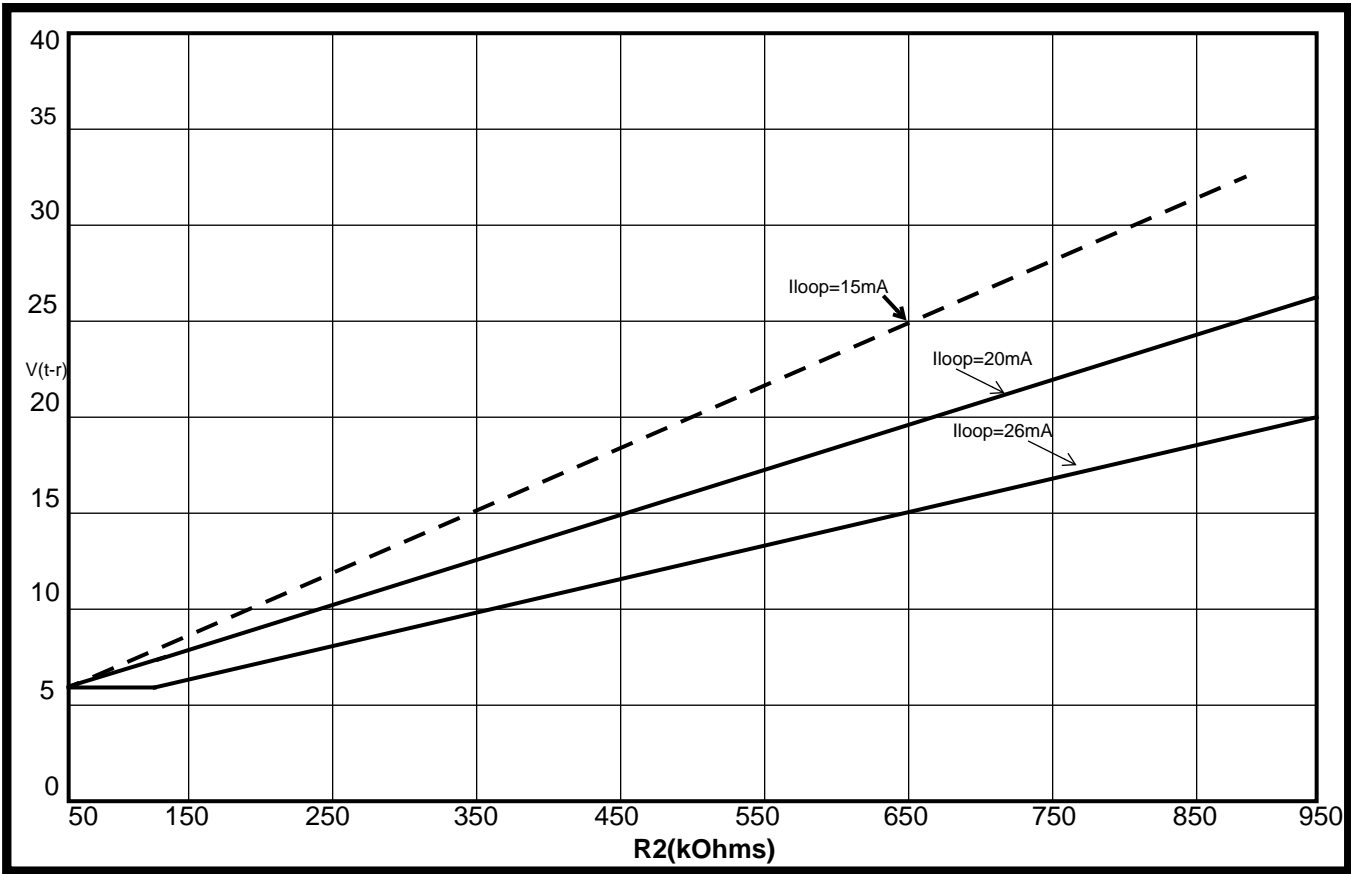


Figure 3 - DC Programming Capability

By applying a logic 0 to Pin 17, \overline{CL} , the loop current will be limited to below 60mA as required in France and the European TBR21 specification. For all other countries where current limiting is not required, \overline{CL} should be set to 1.

The AC input impedance should be set by the user to match the line impedance.

Input Impedance

The MH88437 has a programmable input impedance set by fitting external components between the ZA pin and AGND.

For complex impedances the configuration shown in Figure 4 (below) is most commonly found.

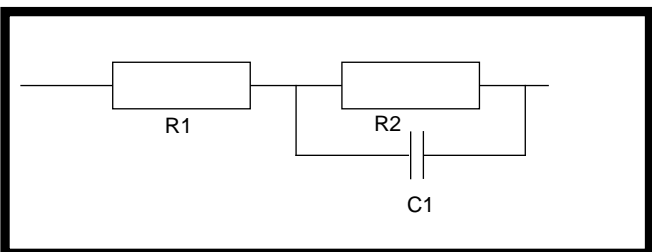


Figure 4 - Complex Impedances

To find the external programming components for configuration, the following formula should be used:

$$Z_{ext} = [(10 \times R1) - 1k3] + [(10 \times R2) // (C1/10)]$$

e.g. If the required input impedance = $220\Omega + (820\Omega // 115nF)$, the external network to be connected to ZA will be:

$$Z_A = 900\Omega + (8k2\Omega // 12nF)$$

Where the input impedance (Z) = 600R the equation can be simplified to:

$$Z_A = (10 \times Z) - 1k3\Omega$$

$$Z_A = 4k7\Omega$$

Note: A table of commonly used impedances can be found in the DAA Application's document MSAN-154.

Where Z_{ext} = external network connected between ZA and AGND and $Z_{int} = 1.3k\Omega$ (internal resistance).

Network Balance

The network balance impedance of the device can be programmed by adding external components between NB1 and NB2. For countries where the balance impedance matches the line impedance, a 16k Ω resistor should be added between NB1 and NB2.

Ring Voltage Detection

The sensitivity of the ringing voltage detection circuitry can be adjusted by applying an external resistor (R7, Figure 5) between the RS and LOOP pins. With a short circuit, the threshold sensitivity is ~10Vrms, therefore $R7 = 30k\Omega \times (\text{Desired threshold voltage} - 10Vrms)$.

Example: 300k Ω gives ~20Vrms and 600k Ω gives ~30Vrms.

An AC ringing voltage across Tip and Ring will cause RV to output TTL pulses at the ringing frequency, with an envelope determined by the ringing cadence.

Parallel Phone and Dummy Ringer

An external parallel phone or dummy ringer circuit can be connected across Tip and Ring as shown in Figure 5. A Dummy Ringer is an AC load which represents a telephone's mechanical ringer.

In normal circumstances when a telephone is On-Hook and connected to the PSTN, its AC (Ringer) load is permanently presented to the network. This condition is used by many PTT's to test line continuity, by placing a small AC current onto the line and measuring the voltage across tip (A) and ring (B).

Today's telecom equipment may not have an AC load present across tip and ring (e.g. modems), therefore any testing carried out by the PTT will see an open circuit across tip and ring. In this instance the PTT assumes that the line continuity has been damaged.

To overcome this problem many PTT's specify that a "Dummy Ringer" is presented to the network at all times. Ideally its impedance should be low in the audio band and high at the ringing frequencies (e.g. 25Hz). Note that the requirement for the "Dummy Ringer" is country specific.

Parallel phone detection is used mostly in set-top box applications. This is when a modem call will need to be disconnected from the central office by the equipment when the parallel phone is in the off-hook state. This is to allow the subscriber to make emergency calls.

To detect this state, additional circuitry will be required. Refer to Application note MSAN-154.

2-4 Wire Conversion

The device converts the balanced 2-Wire input, presented by the line at Tip and Ring, to a ground referenced signal at VX, biased at 2.0V. This simplifies the interface to a modem chip set.

Conversely, the device converts the differential signal input at VR+ and VR- to a balanced 2-Wire signal at Tip and Ring. The device can also be used in a single ended mode at the receive input, by leaving VR+ open circuit and connecting the input signal to VR- only. Both inputs are biased at 2.0V.

During full duplex transmission, the signal at Tip and Ring consists of both the signal from the device to the line and the signal from the line to the device. The signal input at VR+ and VR- being sent to the line, must not appear at the output VX. In order to prevent this, the device has an internal cancellation circuit, the measure of this attenuation is Transhybrid Loss (THL).

The MH88437 has the ability to transmit analog signals from Tip and Ring through to VX when on-hook. This can be used when receiving caller line identification information.

Transmit Gain

The Transmit Gain of the MH88437 is the gain from the differential signal across Tip and Ring to the ground referenced signal at VX. The internal Transmit Gain of the device is fixed as shown in the AC Electrical Characteristics table. For the correct gain, the Input Impedance of the MH88437, must match the specified line impedance.

By adding an external potential divider to VX, it is possible to reduce the overall gain in the application. The output impedance of VX is approximately 10 Ω and the minimum resistance from VX to ground should be 2k Ω .

Example: If $R3 = R4 = 2k\Omega$, in Figure 5, the overall gain would reduce by 6.0dB.

Receive Gain

The Receive Gain of the MH88437 is the gain from the differential signal at VR+ and VR- to the differential signal across Tip and Ring. The internal Receive Gain of the device is fixed as shown in the AC Electrical Characteristics table. For the correct gain, the Input Impedance of the MH88437 must match the specified line impedance.

With an internal series input resistance of $47k\Omega$ at the VR+ and VR- pins, external series resistors can be used to reduce the overall gain.

Overall Receive Gain = $0dB + 20\log(47k\Omega / (47k\Omega + R5))$.

For differential applications R6 must be equal to R5 in Figure 5.

Example: If $R5 = R6 = 47k$ in Figure 3, the overall gain would reduce by 6.0dB.

Supervisory Features

The device is capable of monitoring the line conditions across Tip and Ring, this is shown in Figure 5. The Loop Condition Detect pin (LCD), indicates the status of the line. The LCD output is at logic 1 when loop current flows, indicating that the MH88437 is in an off hook state. LCD will also go high if a parallel phone goes off-hook. Therefore, line conditions can be determined with the LC and the LCD pins.

The LOOP pin output voltage VLOOP is proportional to the line voltage across Tip and Ring scaled down by a factor of 50 and offset by 2.0V(t-r). With the aid of a simple external detector the LC, LCD and LOOP pins can be used to generate the signals necessary for parallel phone operation, e.g. with a Set Top Box. See MSAN-154 for further details.

When the device is generating dial pulses, the LCD pin outputs TTL pulses at the same rate. The LCD output will also pulse if a parallel phone is used to dial and when ringing voltage is present at Tip and Ring.

Mechanical Data

See Figures 12, 13 and 14 for details of the mechanical specification.

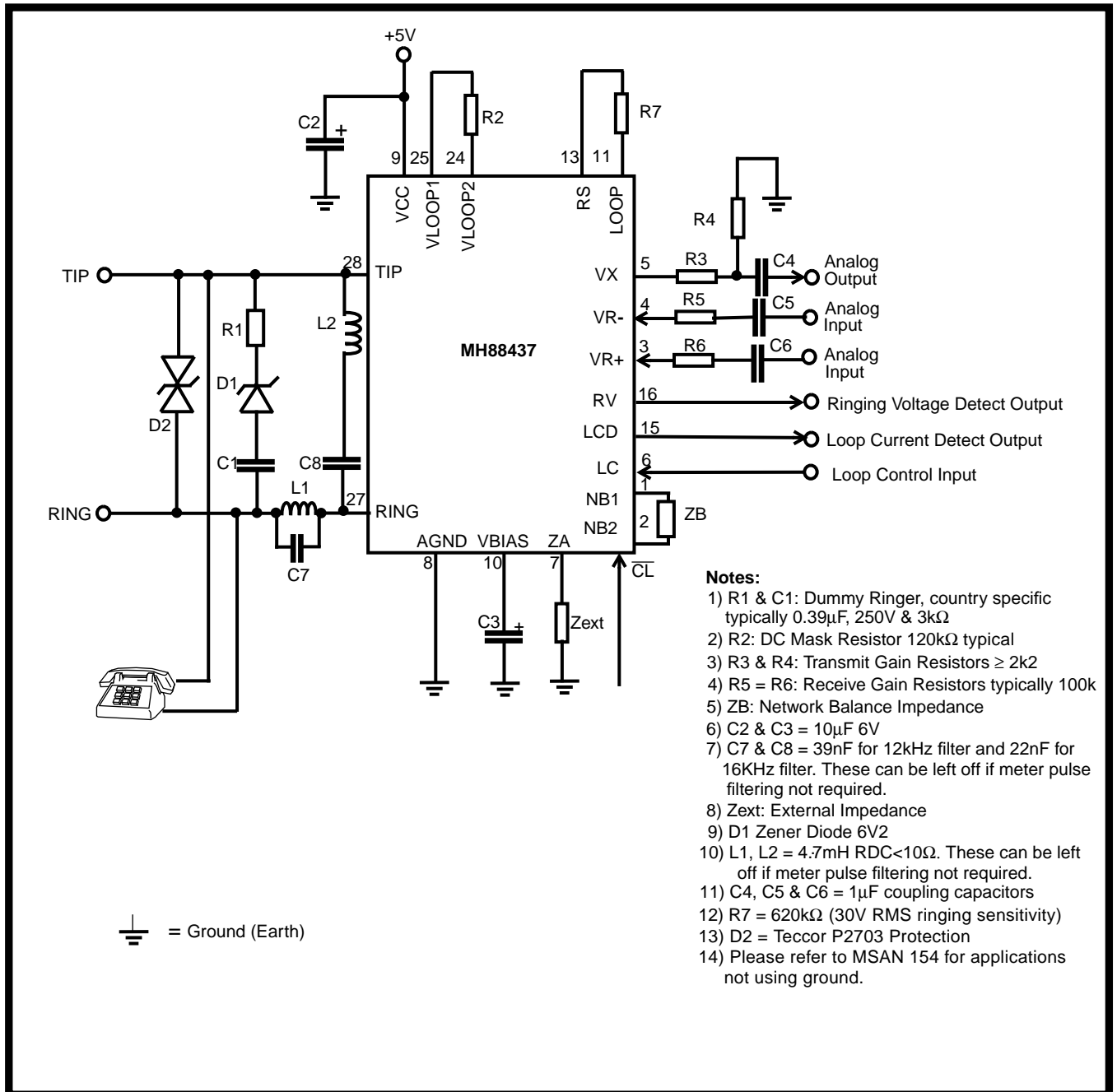


Figure 5 - Typical Application Circuit

Absolute Maximum Ratings* - All voltages are with respect to AGND unless otherwise specified.

	Parameter	Sym	Min	Max	Units	Comments
1	DC Supply Voltage	V _{CC}	-0.3	6	V	
2	Storage Temperature	T _S	-55	+125	°C	
3	DC Loop Voltage	V _{TR}	-110	+110	V	
4	Transient loop voltage	V _{TR}		300	V	1ms On hook
5	Ringing Voltage	V _R		130	V _{rms}	V _{BAT} = -56V
6	Loop Current	I _{Loop}		60 90	mA mA	$\overline{CL}=0$ V _{TIP-RING} ≤40V $\overline{CL}=1$
7	Ring Trip Current	I _{TRIP}		180	mA _{rms}	250ms 10% duty cycle or 500ms single shot

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions

	Parameter	Sym	Min	Typ [‡]	Max	Units	Test Conditions
1	DC Supply Voltages	V _{CC}	4.75	5.0	5.25	V	
2	Operating Temperatures	T _{OP}	0	25	70	°C	
3	Ringing Voltage	V _R		75	90	V _{rms}	V _{BAT} = -48V

‡ Typical figures are at 25°C with nominal +5V supply and are for design aid only

Loop Electrical Characteristics † -

	Characteristics	Sym	Min	Typ [‡]	Max	Units	Test Conditions
1	Ringing Voltage No Detect Detect	V _R			7 14	V _{rms} V _{rms}	Externally Adjustable
2	Ringing Frequency		15		68	Hz	
3	Operating Loop Current		15		60 80	mA mA	$\overline{CL}=0$ V _{TIP-RING} ≤40V $\overline{CL}=1$ Note 1
4	Off-Hook DC Voltage				6.0 6.0 7.8	V V V	Externally Adjustable I _{Loop} =15mA) I _{Loop} =20mA) Note 3 I _{Loop} =26mA) where R2 = 110kΩ
5	Leakage Current (Tip or Ring to AGND)				10 7	μA mA	100V DC Note 2. 1000V AC
6	Leakage Current on-hook (Tip to Ring)			9 18	10 20	μA	V _{BAT} (= -50V) V _{BAT} (= -100V)
7	Dial Pulse Detection ON OFF		0 0	+1 +1	+4 +4	ms ms	Dial pulse delay
8	Loop Condition Detect Threshold Off-Hook		5		16	V	Voltage across tip and ring

† Electrical Characteristics are over Recommended Operating Conditions unless otherwise stated.

‡ Typical figures are at 25°C with nominal +5V supplies and are for design aid only.

Note 1: Low Loop current operation depends on value of resistor connected between V_{Loop} 1 and V_{Loop} 2.

Note 2: This is equivalent to 10MΩ leakage Tip/Ring to Ground.

Note 3: Refer to EIA/TIA 464 Section 4.1.1.4.4

DC Electrical Characteristics †

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1		Supply Current	I_{CC}		5		mA	V_{DD} (= 5.0V, On-hook)
2	RV, LCD	Low Level Output Voltage High Level Output Voltage	V_{OL} V_{OH}	2.4		0.4	V V	$I_{OL} = 4mA$ $I_{OH} = 0.4mA$
3	LC	Low Level Input Voltage High Level Input Voltage Low Level Input Current High Level Input Current	V_{IL} V_{IH} I_{IL} I_{IH}	2.0	0 350	0.8 60 400	V V μA μA	$V_{IL} = 0.0V$ $V_{IH} = 5.0V$
4	VR+ VR-	DC common mode	VCM	0	2	VCC	VDC	Use coupling caps for higher voltages and single ended

† Electrical Characteristics are over Recommended Operating Conditions unless otherwise stated.

‡ Typical figures are at 25°C with nominal + 5V supplies and are for design aid only.

AC Electrical Characteristics †

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1		Input Impedance VR- VR+			47k 94k		Ω Ω	
2		Output Impedance at VX			10		Ω	
3		Receive Gain (VR to 2-Wire)		-1	0	1	dB	Test circuit as Fig 8 Input 0.5V at 1kHz
4		Frequency Response Gain (relative to Gain @ 1kHz)		-0.5	0	0.5	dB	$I_{LOOP} = 15-60mA$ 300Hz to 3400 Hz
5		Signal Output Overload Level at 2-Wire at VX			0 0		dBm dBm	THD $\leq 5\%$ @ 1kHz $I_{LOOP} = 25-60mA$ VCC = 5V
6		Signal/Noise & Distortion at 2-Wire at VX	SINAD		70 70		dB dB	Input 0.5V at 1kHz $I_{LOOP} = 25-60mA$ 300-3400Hz
7		Power Supply Rejection Ratio at 2-Wire at VX	PSRR	25 25	40 40		dB dB	Ripple 0.1Vrms 1kHz on V_{DD}
8		Transhybrid Loss	THL	16	25		dB	Test circuit as Fig 8 300-3400Hz at V_R
9		2-Wire Input Impedance	Zin		Note 3		Ω	@ 1kHz
10		Return Loss at 2-Wire (Reference 600 Ω)	RL	14 20 18	24 24 24		dB dB dB	Test circuit as Fig 9 200-500Hz 500-2500Hz 2500-3400Hz
11		Longitudinal to Metallic Balance Metallic to Longitudinal Balance	Nc	46 46 60 40	58 53		dB dB dB dB	Test circuit as Fig. 10 300-1000Hz 1000-3400Hz Test circuit as Fig. 11 200-1000Hz 1000-4000Hz

AC Electrical Characteristics † (continued)

	Characteristics	Sym	Min	Typ [‡]	Max	Units	Test Conditions
12	Idle Channel Noise at 2-Wire at VX at 2-Wire at VX			15 15 -65 -65	20 20	dBrnC dBrnC dBm dBm	Cmess filter 300-3400Hz filter
13	Transmit Gain (2-Wire to VX) Off-Hook On-Hook		-1	0 0	+1	dB dB	Test circuit as Fig 7 Input 0.5V @ 1kHz LC = 0V
14	Frequency Response Gain (relative to Gain @ 1kHz)		-0.5 -0.5	0 0	0.5 0.5	dB dB	300Hz 3400Hz
15	Intermodulation Distortion products at VX and 2W	IMD		75		dB	I _{LOOP} = 25-60mA F1 = 1kHz at -6dBm F2 = 800Hz at -6dBm Total signal power = -3dBm
16	Distortion at VX due to near end echo (300Hz - 3400Hz bandwidth)			75		dB	I _{LOOP} = 25-60mA F1 = 1kHz at -6dBm F2 = 800Hz at -6dBm Total signal power = -3dBm
17	Common Mode Rejection at VX	CMR		50		dB	Test circuit as Fig 10 1-100Hz Note 4
18	Common Mode overload	CML		100V		V _{pk-pk}	Test circuit as Fig 10 1-100Hz Note 4

† Electrical Characteristics are over Recommended Operating Conditions unless otherwise stated.

‡ Typical figures are at 25°C with nominal +5V and are for design aid only.

Note 1: All of the above test conditions use a test source impedance which matches the device's impedance.

Note 2: dBm is referenced to 600Ω unless otherwise stated.

Note 3: These parameters need to be taken into consideration when designing the power supply.

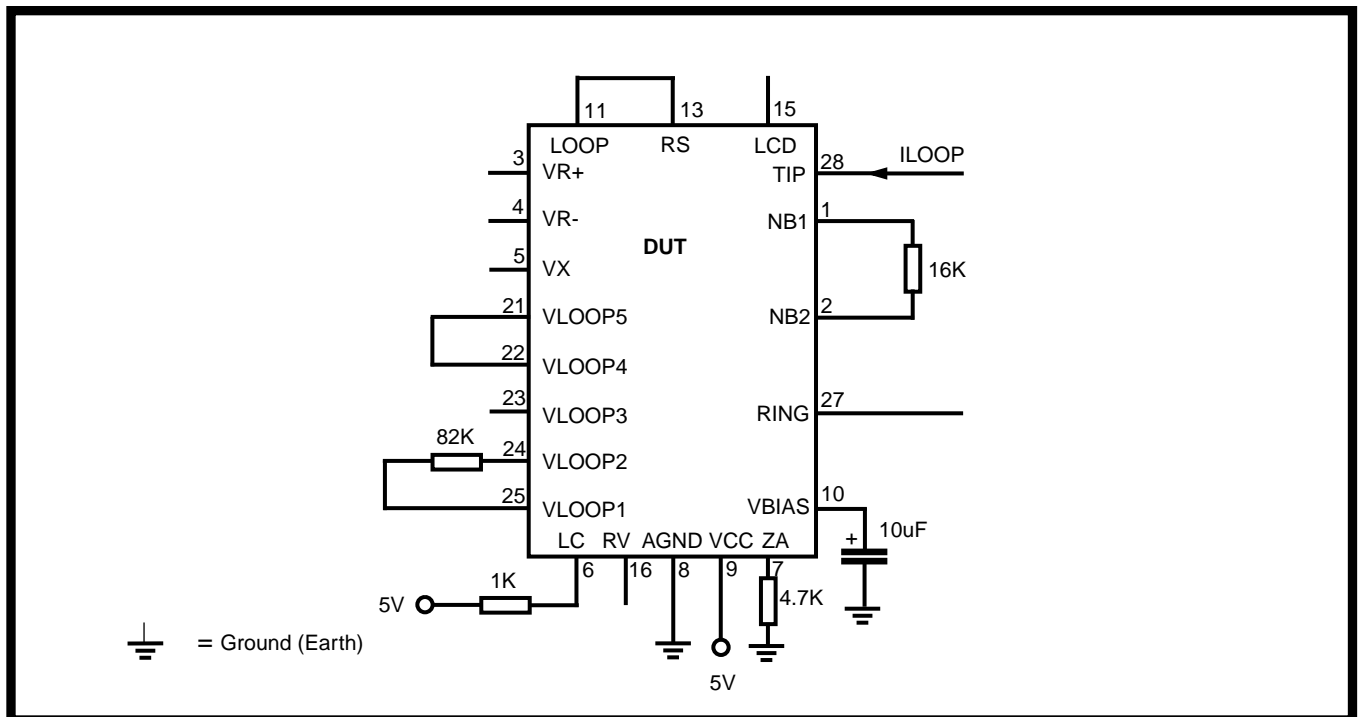


Figure 6 - Test Circuit 1

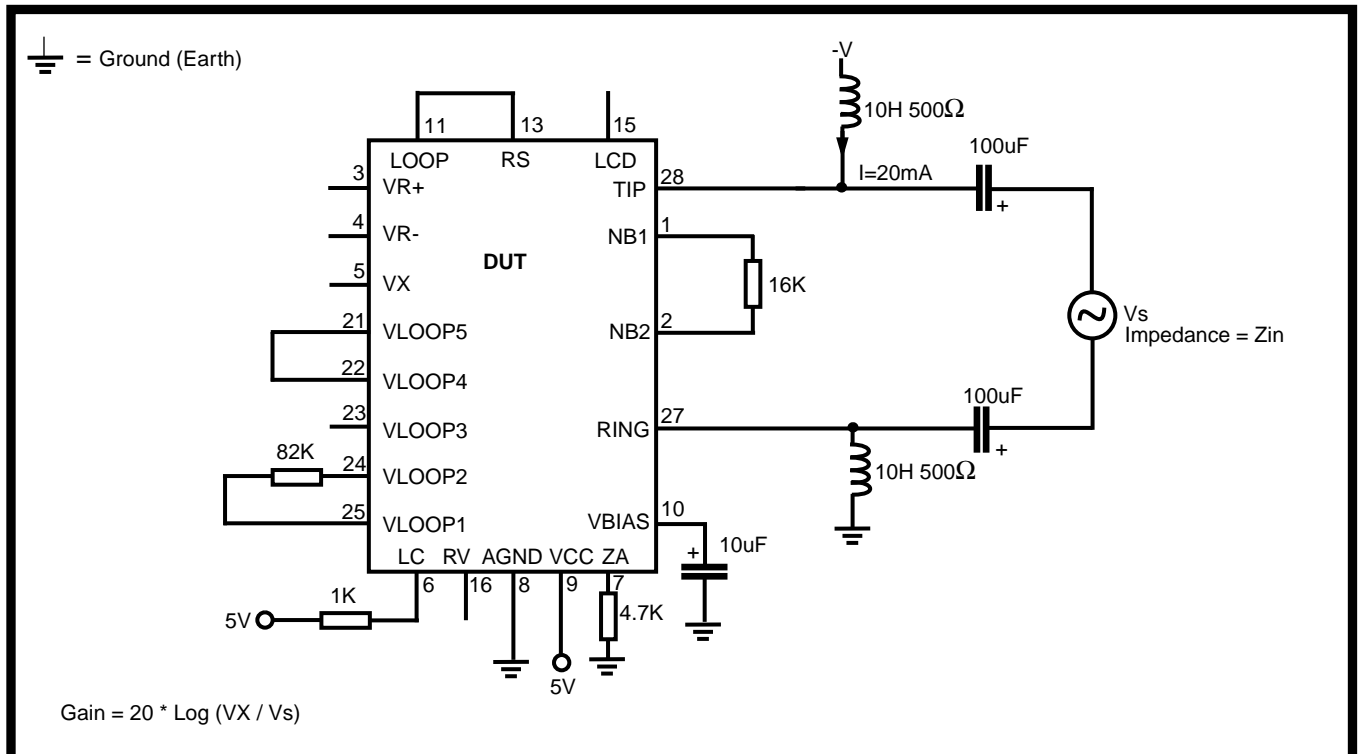


Figure 7 - Test Circuit 2

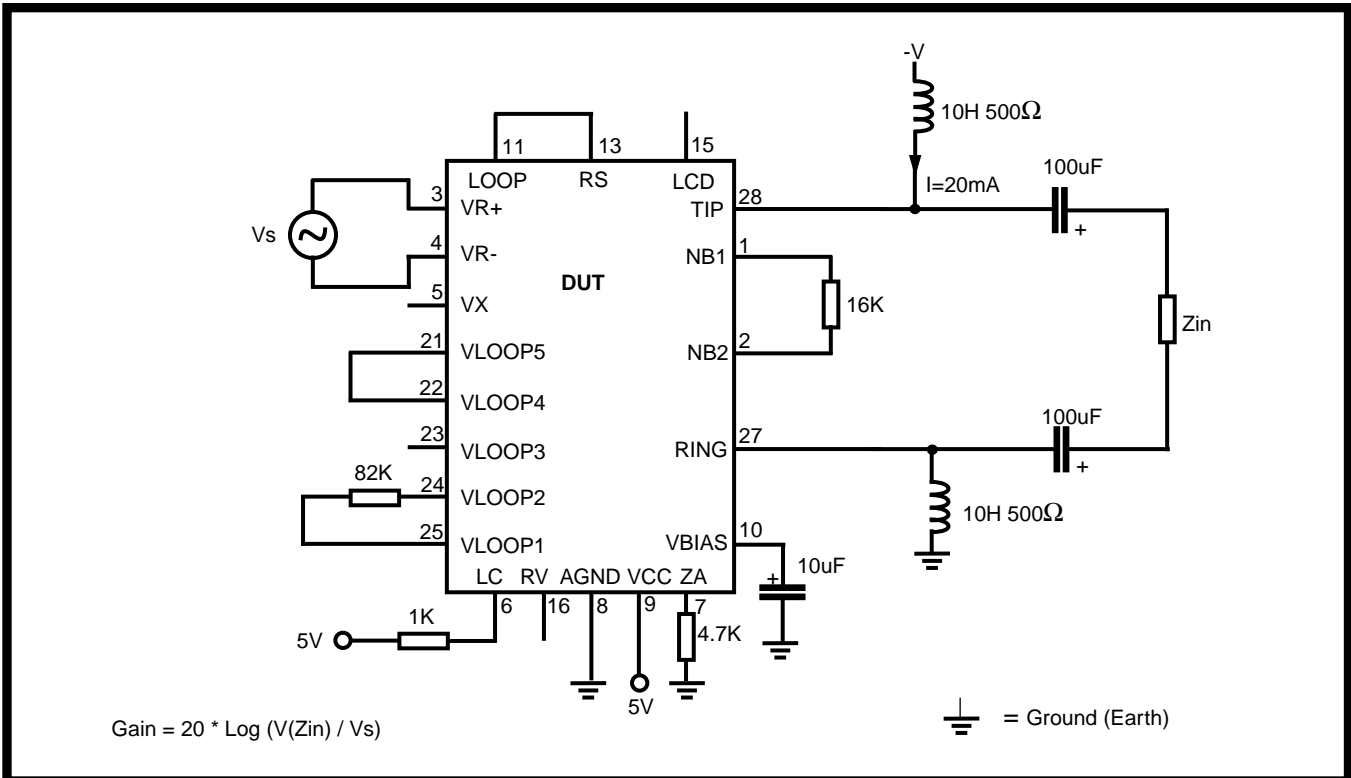


Figure 8 - Test Circuit 3

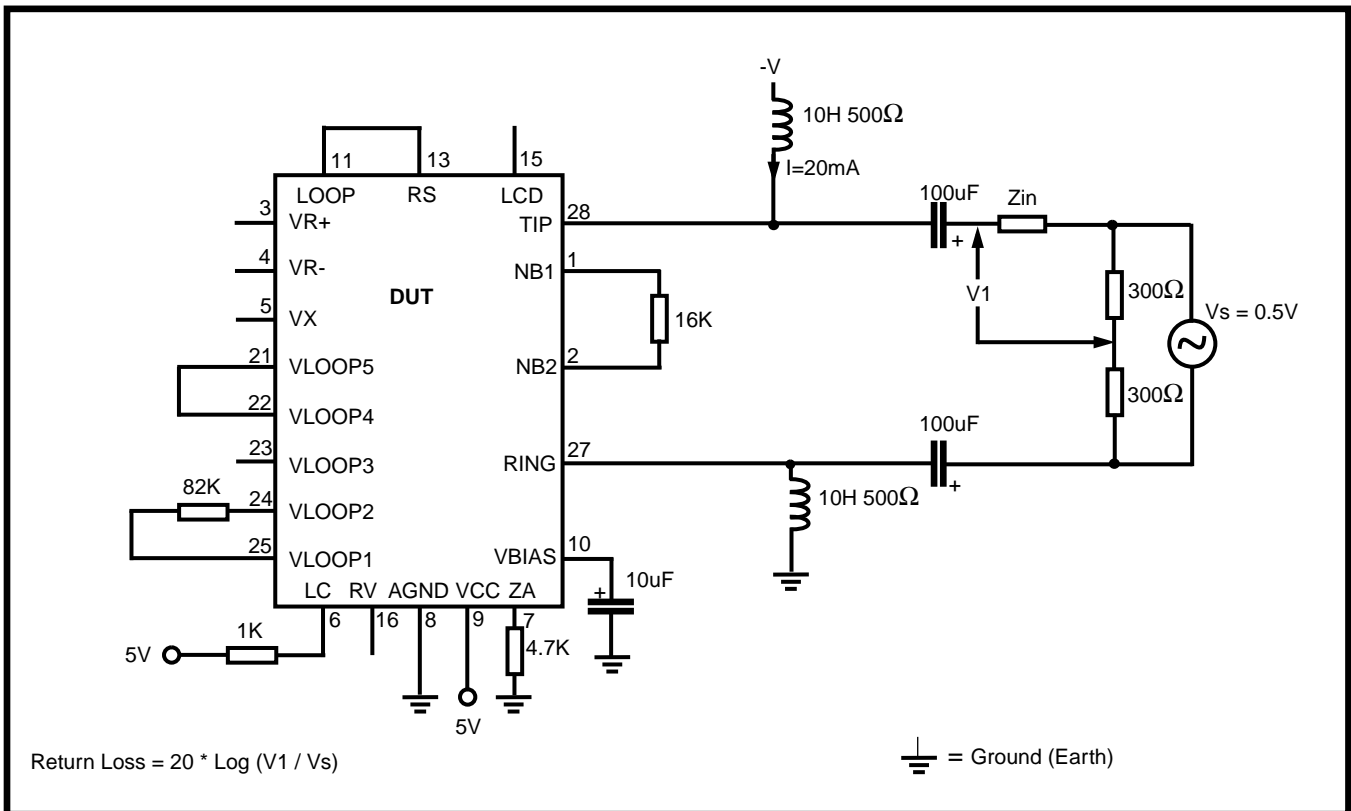


Figure 9 - Test Circuit 4

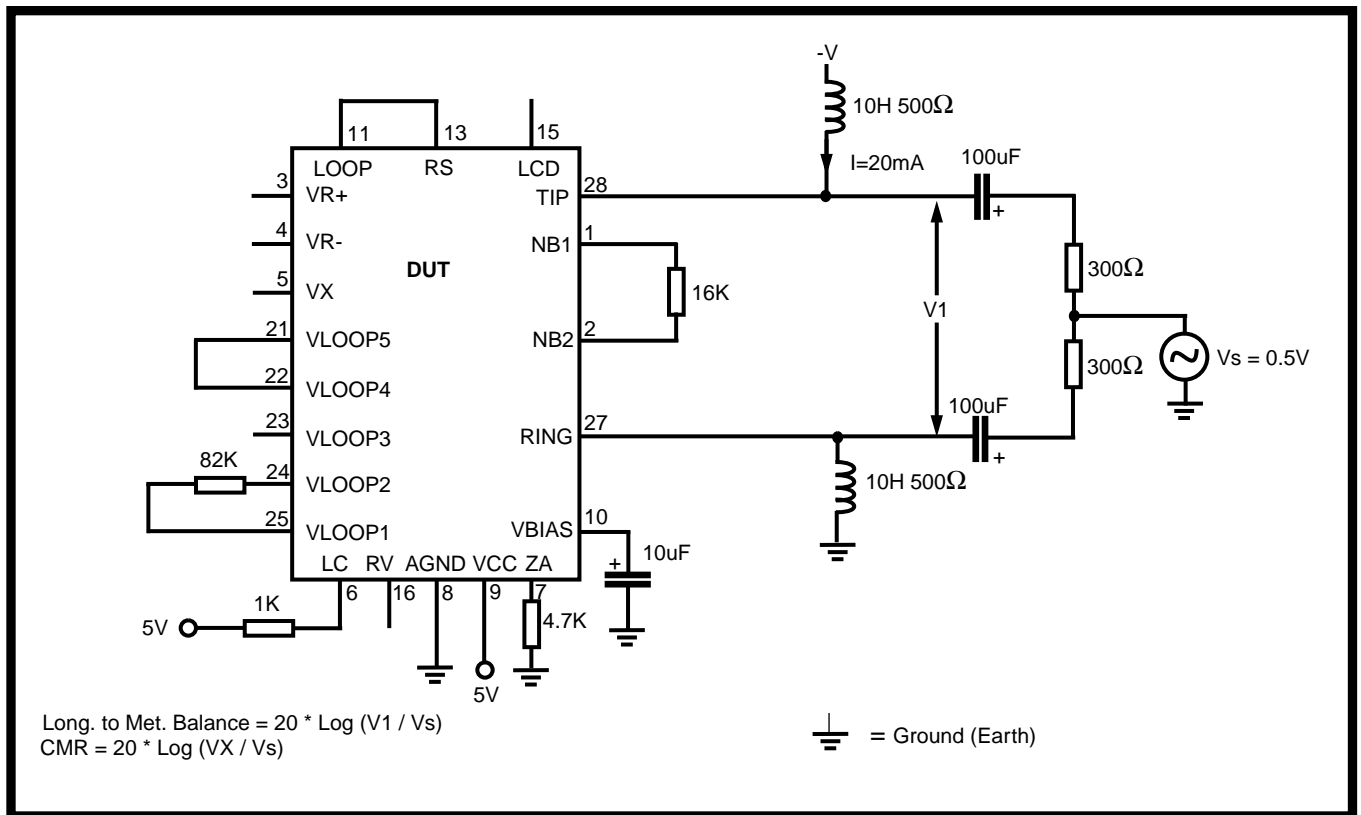


Figure 10 - Test Circuit 5

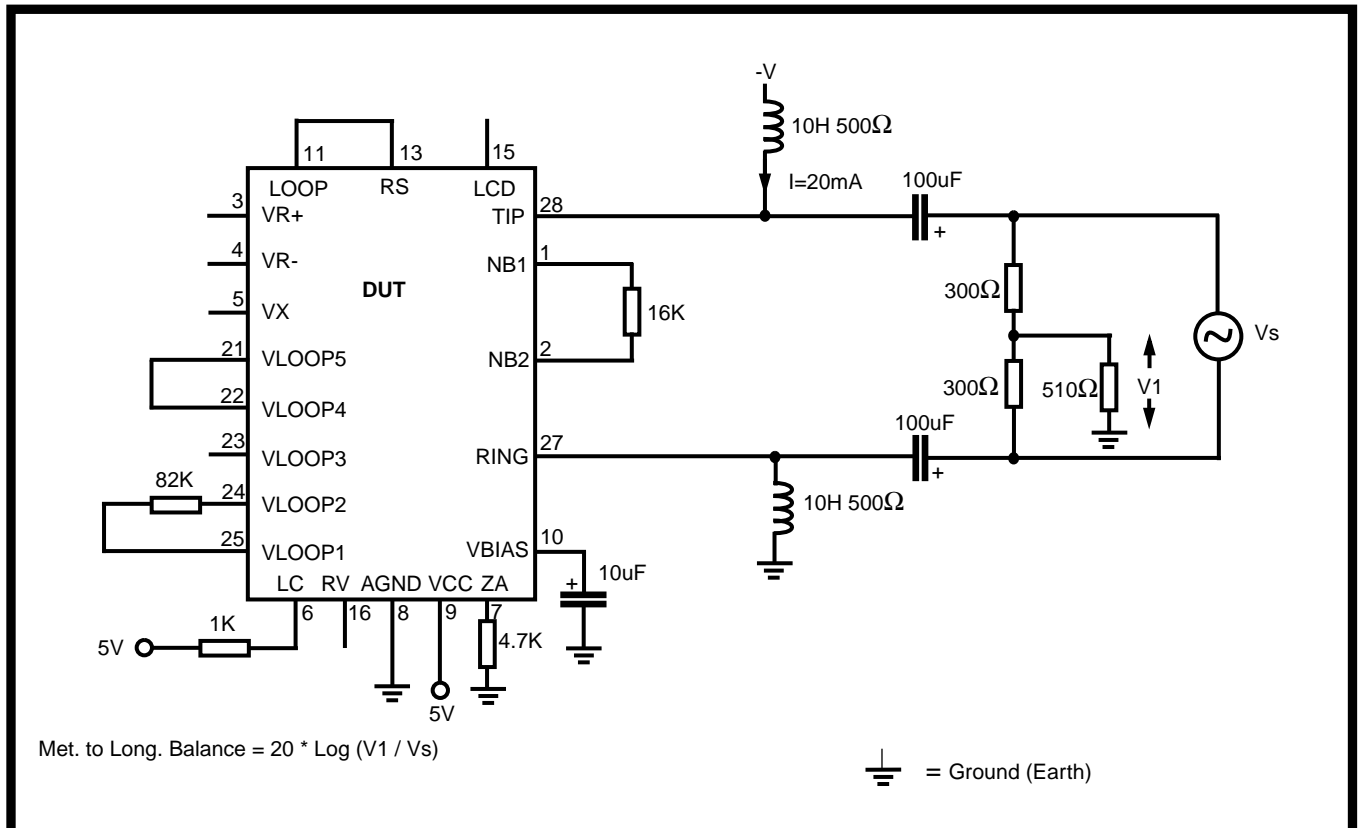


Figure 11 - Test Circuit 6

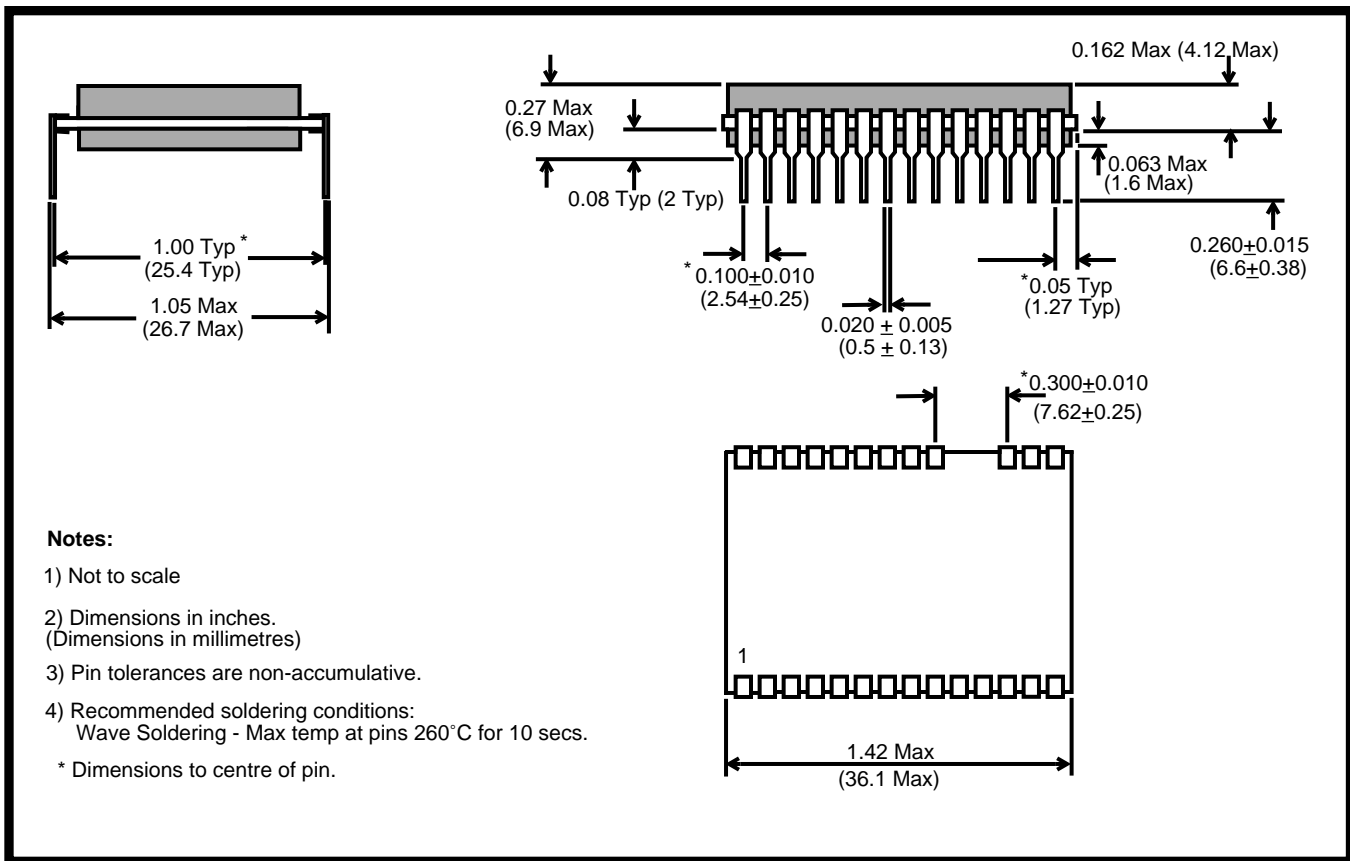


Figure 12 - Mechanical Data for 28 Pin DIL Hybrid

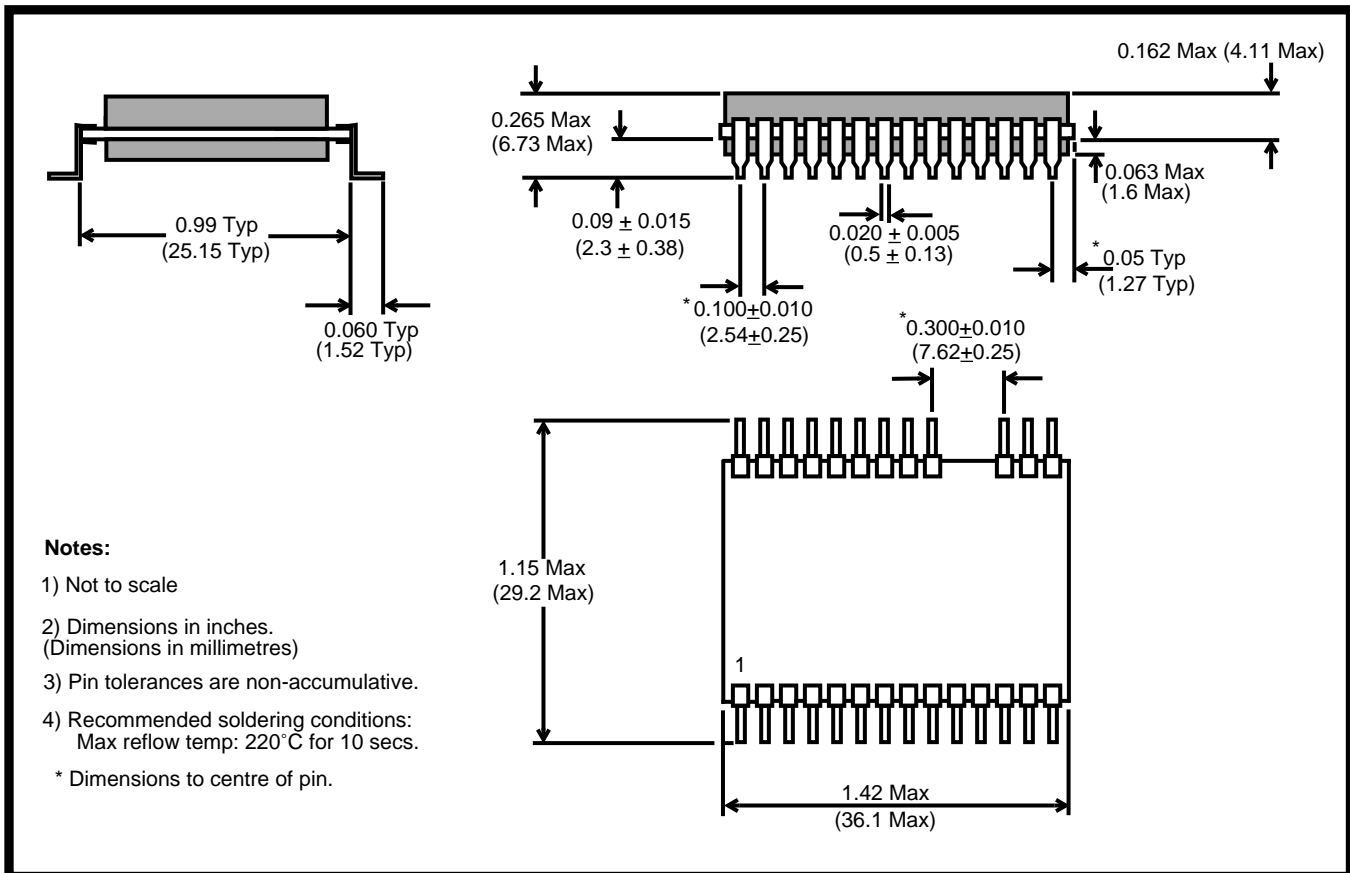


Figure 13 - Mechanical Data for 28 Pin Surface Mount Hybrid

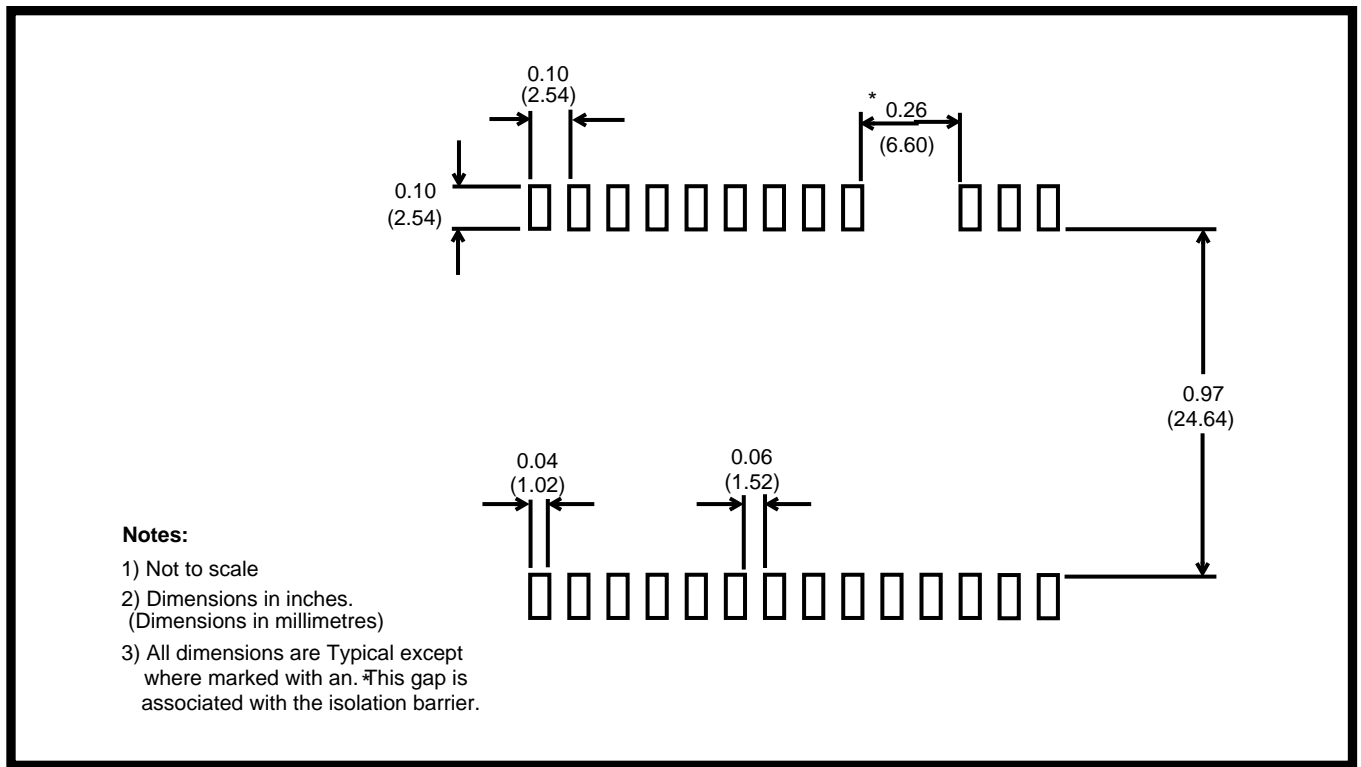


Figure 14 - Recommended Footprint for 28 Pin Surface Mount Hybrid

Notes: